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(19)(CA) **APPLICATION FOR CANADIAN PATENT** (12)

(54) Power Supply Control Circuit

(72) Uehara, Toshiyuki - Japan ;

(71) Mitsubishi Denki Kabushiki Kaisha - Japan ;

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(57) 6 Claims

POWER SUPPLY CONTROL CIRCUIT

ABSTRACT OF THE DISCLOSURE:

In supplying power to a group of peripheral devices of a processor, a power supply control circuit supplies power only to a peripheral device that is being accessed by the processor, stops power supply to a peripheral device that is not being accessed by the processor, or supplies power only to a peripheral device designated by the processor in accordance with an operation mode of the processor. A power supply control circuit comprises a decoder circuit which selects a peripheral device that is being accessed by a processor, or a selector circuit which selects a peripheral device designated by the processor; power switches of each peripheral device which input a power supply selection signal of peripheral device to be power supplied; and a processor peripheral circuit. Thus, it is possible to optionally determine or select power supply to a group of peripheral devices of a processor and to realize reduction in electricity consumption by a peripheral device circuit of the processor by a simple circuit structure.

POWER SUPPLY CONTROL CIRCUIT

INDUSTRIAL USE OF THE INVENTION:

The present invention relates to a power supply control circuit for controlling the supply of power to peripheral devices by processor control.

PRIOR ART

Fig. 1 is a block diagram showing the prior art power supply control circuit, wherein the numeral 1 denotes a processor; 2 a system bus for the processor; 4 a driver for the system bus of the processor; 5 - 7 peripheral devices Dev[1] - Dev[r] - Dev[n] ($1 \leq r \leq n$: n is a positive integer) to be connected to the system bus of the processor; 9 a supply power source.

Next, an operation of the prior art circuit will be explained.

In Fig. 1, in order to access the device designated in accordance with an instruction from a program, processor 1 sends via system bus 2 a command necessary for selecting the device to peripheral devices 5 - 7 directly connected to bus driver 4, whereby processor 1 accesses the device designated by the program.

While the processor is operating, supply power source 9 continues to constantly provide current from the power source to peripheral devices Dev[1] - Dev[r] - Dev[n] regardless of whether or not the processor is accessing the peripheral devices for data.

Due to the aforementioned constitution of the prior art power control circuit, power is constantly supplied to peripheral devices irrespective of various operation modes of a processor, which leads to a large amount of power consumption.

The object of the present invention is to obviate the aforementioned problems of the prior art and to provide an efficient power supply control circuit free from wasteful power consumption by exercising control to supply power or stop supplying power to peripheral devices in accordance with various operation modes of a processor.

SUMMARY OF THE INVENTION:

According to the present invention, a power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprises means which generates a selection signal for selecting a designated peripheral device based on command data outputted from the processor; and a group of power switch means which are respectively connected to the group of peripheral devices and turn on or off power to be supplied from the power source to the designated peripheral device in response to the selection signal.

Furthermore, according to the present invention, a power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprises means which inputs a peripheral device indication signal outputted from the processor for designating a peripheral device to which power is to be

supplied regardless of whether or not the processor is accessing the peripheral devices and an enable signal for determining whether the peripheral device indication signal is active (on) or non-active (off), and then outputs a power supply indication signal for indicating power supply to the peripheral device designated when the peripheral device indication signal is active (on); means for outputting a selector·reset signal which indicates, in response to a port output signal outputted from the processor at a predetermined timing, whether the signal is active (on) or non-active (off); selector means which is connected to the means for outputting a power supply indication signal and to the means for outputting a selector·reset signal, and outputs a power supply selection signal when the selector·reset signal is non-active (off); and a group of power switch means which are respectively connected to the group of peripheral devices, and turn on or off power to be supplied from the power source to the designated peripheral device in response to the power supply selection signal.

Still further, according to the present invention, a power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprises at least one pattern generator means which generates a power supply pattern selection signal for the peripheral devices in response to a pattern indication signal outputted from the processor which designates an on/off pattern of power to be supplied to a peripheral device, regardless of whether the processor is accessing

the peripheral devices; means for generating a power supply selection signal in response to the pattern selection signal; and a group of power switch means which are respectively connected to the group of peripheral devices, and turn on or off power to be supplied from the power source to the pattern-designated peripheral device in response to the power supply selection signal.

Still further, according to the present invention, a power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprises a pattern generator means which is provided with a command register corresponding to combination patterns of power supply to the peripheral devices, and generates a power supply selection signal concerning a designated peripheral device based on command data outputted from the processor; and a group of power switch means respectively connected to the group of peripheral devices which turn on or off power to be supplied from the power source to the designated peripheral device in response to the power supply selection signal.

A power supply control circuit of the present invention operates in such a manner that a power switch for supplying power to a peripheral device is controlled to be turned on or off in accordance with command data sent from a processor, whereby it is possible to supply power exclusively to a peripheral device that is being accessed by the processor.

Furthermore, a power supply control circuit of the present invention selects an optional peripheral device that is being accessed on the basis of command data from a processor and controls a timing to turn on or off power to be supplied to the thus selected peripheral device irrespective of the command data from the processor.

Still further, a power supply control circuit of the present invention is capable of optionally designating a peripheral device according to the output results of a combination of a plurality of pattern generators.

The present invention pertains to a power supply control circuit which supplies power exclusively to a peripheral device that is being accessed by a processor and stops supplying power to other peripheral devices which are not being accessed or have already been accessed by the processor, whereby it is possible to curtail wasteful consumption of power.

Furthermore, a power supply control circuit according to the present invention always selects only a peripheral device that is being accessed by a processor and controls a timing to turn on or off power to the peripheral device in accordance with command data from the processor regardless of whether the device is being accessed by the processor, whereby it is possible to exercise a specific control to turn on or off power.

Still further, a power supply control circuit according to the present invention selects a peripheral device to be accessed as a final object by combination of

a plurality of pattern generator circuits, whereby it is possible to classify a plurality of groups of peripheral devices to which power is to be supplied in accordance with control content of a program or to divide the same in accordance with hierarchical structure.

BRIEF EXPLANATION OF THE DRAWINGS:

Fig. 1 is a block diagram showing the prior art power supply control circuit in the periphery of a processor.

Fig. 2 is a block diagram showing a power supply control circuit in the periphery of a processor according to Embodiment 1 of the present invention.

Fig. 3 is a block diagram showing a power supply control circuit in the periphery of a processor according to Embodiment 2 of the present invention.

Fig. 4 is a block diagram showing a power supply control circuit in the periphery of a processor according to Embodiment 3 of the present invention.

Fig. 5 is a block diagram showing a power supply control circuit in the periphery of a processor according to Embodiment 4 of the present invention.

Fig. 6 is a block diagram showing a power supply control circuit in the periphery of a processor according to Embodiment 5 of the present invention.

EMBODIMENTS:

Hereinafter, Embodiment 1 of the present invention will be explained by way of Fig. 2.

In Fig. 2, the numeral 1 denotes a processor; 2 a system bus for the processor; 3 a decoder for decoding an address from the system bus and for turning active only a peripheral device selection signal for a peripheral device which is being accessed by the processor; 4 a driver for the system bus of the processor; 5 - 7 peripheral devices Dev[1] - Dev[r] - Dev[n] ($1 \leq r \leq n$: n is a positive integer) to be connected to the system bus of the processor; 8 a power source switch; 9 a power supply source; 10 an enable signal from the processor; 11 - 13 a selection signal for supplying power to a peripheral device.

Next, an operation of the present circuit will be explained. The following explanation is based on the case where a processor selects peripheral device 6.

First, processor 1 sends out via system bus 2 and bus driver 4 command data required for designating a peripheral device to be accessed among peripheral devices 5 - 7.

Next, upon receipt of enable signal 10 from processor 1, decoder 3 turns active (on) a selection signal for supplying power to a peripheral device when a CPU write cycle starts after processor initialization.

More specifically, peripheral device selection signal 12 for power switch 8 of peripheral device Dev[r]6 is turned active, while selection signals 11 - 13 for power supply switches 8 of Dev[1]5 - Dev[n]7 but Dev[r]6 are turned non-active.

As a result, peripheral device selection signal 12 turns on power switch 8, whereby power is supplied to peripheral device Dev[r]6 and bus driver 4 connected thereto.

On the other hand, peripheral device selection signals 11 - 13 but peripheral device selection signal 12 turn off power switches 8 of Dev[1]5 - Dev[n]7 but Dev[r]6, whereby power supply to Dev[1]5 - Dev[n]7 but Dev[r]6 and to the bus drivers connected to the devices is stopped.

Upon completion of access to Dev[r]6 in the aforementioned manner, decoder 3 turns non-active (off) enable signal 10 from processor 1 in response to the instruction from processor 1 when a CPU write cycle finishes, and then turns non-active (off) peripheral device selection signal 12 for power switch 8 of Dev[r]6 which has been accessed. As a result, peripheral device selection signal 12 turns off power switch 8 and stops supplying power to peripheral device Dev[r]6 and bus driver 4 leading to Dev[r]6.

In a read/write cycle of CPU, enable signal 10 is outputted as a signal accessing CPU, which is synchronized with an output of an address/data signal on system bus 2. Decoder 3 address-decodes an address output signal on system bus 2 outputted while the enable signal remains active (on) to thereby turn active (on) selection signals 11 - 13 of relevant peripheral devices.

Next, Embodiment 2 of the present invention will be explained by way of Fig. 3.

Although Embodiment 1 refers to a power supply control circuit using a special decoder receiving an input from system bus 2 of processor 1 to generate a peripheral device selection signal, as is indicated in Fig. 3, a power supply control circuit provided with selector circuit 15, wherein port output signal 14 from processor 1 becomes a direct input for a selection signal is also capable of accomplishing the same operation as in Embodiment 1.

Selector circuit 15 receives as gate inputs port output signals 14 and enable signal 10, which are outputted from processor 1, the port output signals respectively corresponding to selection signals 11 - 13 of the respective peripheral devices and the enable signal determining whether the port output signals are active or non-active, and then outputs conjunction of the inputted signals as selection signals 11 - 13 for the respective peripheral devices.

Next, Embodiment 3 of the present invention will be explained by way of Fig. 4.

In Fig. 4, peripheral device indication signal 22 from processor 1 and enable signal 10 outputted from processor 1 at a required optional timing are applied to peripheral device selection circuit 17.

In other words, peripheral device indication signal 22 corresponding to peripheral devices 5 - 7 becomes effective while enable signal 10 remain active (on), and peripheral device selection circuit 17 outputs power supply indication signal 20 for selecting only a peripheral device designated by processor 1, regardless of whether or not

processor 1 is accessing peripheral devices 5 - 7.

Since the circuit is designed in such a manner that port output signal 16 outputted from processor 1 at an optional CPU timing is applied to initial reset circuit 18, the initial reset circuit generates selector·reset signal 21 which determines whether the signal is active (on) or non-active (off), irrespective of whether enable signal 10 is active or not.

Next, power supply indication signal 20 and selector·reset signal 21 are applied to selector circuit 19, and then, power supply selection signals 11 - 13 for controlling an ON/OFF status of the designated device are generated.

Thus, by determining in advance the procedure of access to the peripheral devices, power supply to the peripheral devices can be freely controlled at an optional timing required by processor 1.

For example, in the case where processor 1 controls power supply to Dev[r]6, power supply indication signal 20 which turns Dev[r]6 active (on) in response to peripheral device indication signal 22 while enable signal 10 is active (on) is inputted to selector circuit 19.

On the other hand, selector·reset signal 21 which arbitrarily becomes active (on) or non-active (off) when port output signal 16 is inputted to initial circuit 18 is inputted to selector circuit 19 at a CPU timing based on a sequence predetermined by processor 1. As a result, selector circuit 19 turns active (on) selection signal 12

of peripheral device Dev[r]6 designated by power supply indication signal 20, while selector·reset signal 21 remains non-active (off), whereby power supply switch 8 of peripheral device Dev[r]6 is turned on and thus, power is supplied to Dev[r]6.

Next, Embodiment 4 of the present invention will be explained by way of Fig. 5.

In the case where it is possible to preset several on/off patterns of power supply of the peripheral devices, the circuit is provided with special pattern generators 24 and 25 as is indicated in Fig. 5, and power supply pattern selection signals for certain peripheral devices are generated by pattern indication signal 23 from processor 1 by employing a minimum number of interface control signals from the processor, whereas power supply control signals 11 - 13 to be sent to the peripheral devices via pattern selection circuit 26 are further generated, whereby it becomes possible to accomplish power supply control by a simple circuit structure.

For example, in the case where a pattern signal is outputted in such a manner that pattern generator 24 supplies power to peripheral device Dev[r]6, pattern indication signal 23 is first outputted so that processor 1 turns active (on) pattern generator 24. Upon receiving pattern indication signal 23, pattern generator 24 outputs a pattern signal which produces a power supply group including peripheral device Dev[r]6.

Next, pattern selection circuit 26 outputs the result of a logical operation of the pattern signal outputted from pattern generator 24 and the pattern signal of another pattern generator 25 as final selection signals of peripheral devices 11 - 13 to be power-supplied. As a result, only selection signal 12 is turned active (on) and thus, power is supplied only to peripheral device Dev[r]6.

Next, Embodiment 5 of the present invention will be explained by way of Fig. 6.

As is indicated in Fig. 6, the same operation as mentioned above can be performed by a power supply control circuit provided with pattern generator 27 incorporating a command register corresponding to a combination pattern of power supply selection signals 11 - 13 for supplying power to the peripheral devices.

For example, if processor 1 outputs an output command for turning active (on) only Dev[r]6 to pattern generator 27 via system bus 2, pattern generator 27 turns active (on) only peripheral device selection signal 12 in response to the output command and as a result, only power supply selection signal 12 of peripheral device Dev[r]6 is turned active (on) and power is supplied only to peripheral device Dev[r]6.

On the other hand, if processor 1 outputs to pattern generator 27 an output command for turning non-active (off) only peripheral device Dev[r]6 via system bus 2, pattern generator 27 turns non-active (off) only peripheral device selection signal 12 in response to the output command and

as a result, power supply selection signal 12 of peripheral device Dev[r]6 becomes non-active (off), whereby power supply to peripheral device Dev[r]6 is stopped.

The embodiment of the invention in which an exclusive property or privilege are claimed are defined as follows:

1. A power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprising:

means which generates a selection signal for selecting a designated peripheral device based on command data outputted from said processor; and

a group of power switch means which are respectively connected to said group of peripheral devices and turn on or off power to be supplied from said power source to said designated peripheral device in response to said selection signal.

2. A power supply control circuit according to Claim 1, wherein said means for generating a selection signal is a decoder which decodes an address signal from said processor and only turns active (on) a selection signal concerning the designated peripheral device which is being accessed by said processor.

3. A power supply control circuit according to Claim 1, wherein said means for generating a selection signal is a selector circuit which inputs port output signals outputted from said processor respectively corresponding to said group of peripheral devices and enable signals for determining whether the respective port output signals are active (on) or non-active (off), whereby a signal indicating conjunction of such inputted signals is outputted as a selection signal.

4. A power supply control circuit for supplying power

from a power source to a group of peripheral devices connected to a processor, comprising:

means which inputs a peripheral device indication signal outputted from said processor for designating a peripheral device to which power is to be supplied regardless of whether or not said processor is accessing said peripheral devices and an enable signal for determining whether said peripheral device indication signal is active (on) or non-active (off), and then outputs a power supply indication signal for indicating power supply to the peripheral device designated when said peripheral device indication signal is active (on),

means for outputting a selector·reset signal which indicates, in response to a port output signal outputted from said processor at a predetermined timing, whether the signal is active (on) or non-active (off),

selector means which is connected to said means for outputting a power supply indication signal and to said means for outputting a selector·reset signal, and outputs a power supply selection signal when said selector·reset signal is non-active (off); and

a group of power switch means which are respectively connected to said group of peripheral devices, and turn on or off power to be supplied from said power source to said designated peripheral device in response to said power supply selection signal.

5. A power supply control circuit for supplying power from a power source to a group of peripheral devices

connected to a processor, comprising:

at least one pattern generator means which generates a power supply pattern selection signal for said peripheral devices in response to a pattern indication signal outputted from said processor which designates an on/off pattern of power to be supplied to a peripheral device, regardless of whether said processor is accessing said peripheral devices,

means for generating a power supply selection signal in response to said pattern selection signal; and

a group of power switch means which are respectively connected to said group of peripheral devices, and turn on or off power to be supplied from said power source to said pattern-designated peripheral device in response to said power supply selection signal.

6. A power supply control circuit for supplying power from a power source to a group of peripheral devices connected to a processor, comprising:

a pattern generator means which is provided with a command register corresponding to combination patterns of power supply to said peripheral devices, and generates a power supply selection signal concerning a designated peripheral device based on command data outputted from said processor; and

a group of power switch means respectively connected to said group of peripheral devices which turn on or off power to be supplied from said power source to said designated peripheral device in response to said power supply selection signal.

Fig. 1

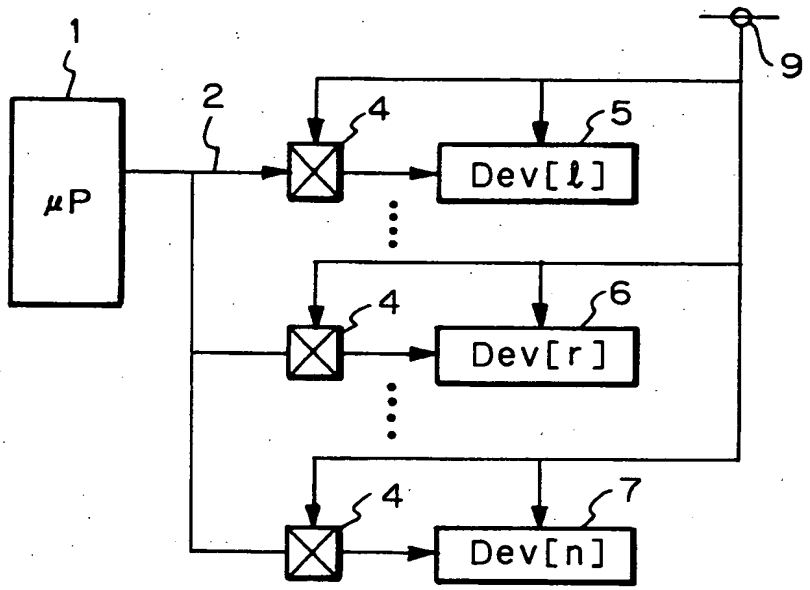
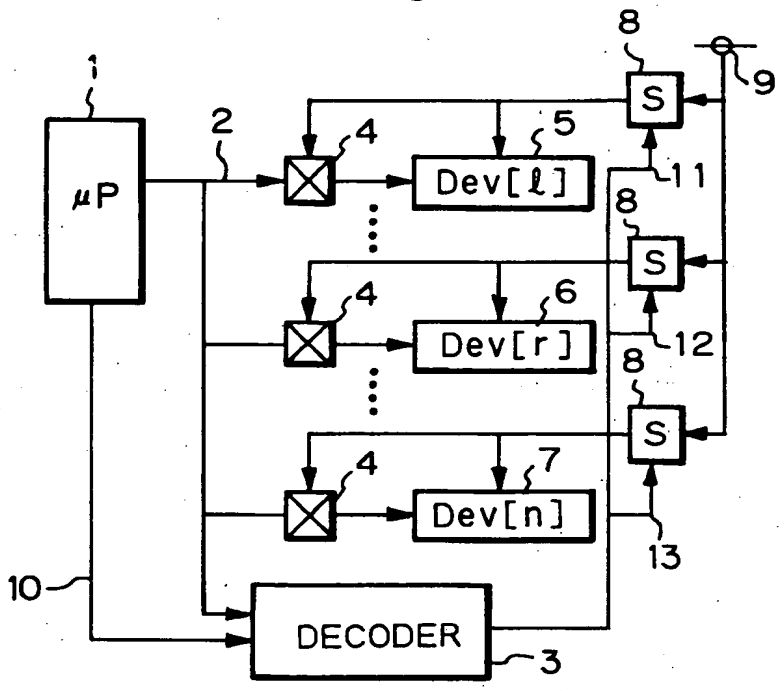


Fig. 2


1
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Dev[ℓ]
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7
Dev[n]
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10
DECODER
3

Fig. 3

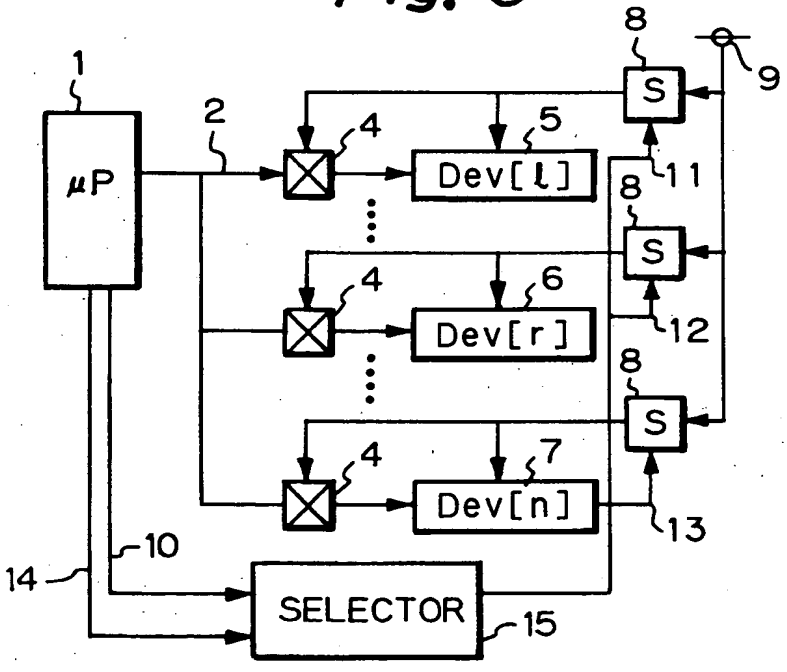
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Fig. 4

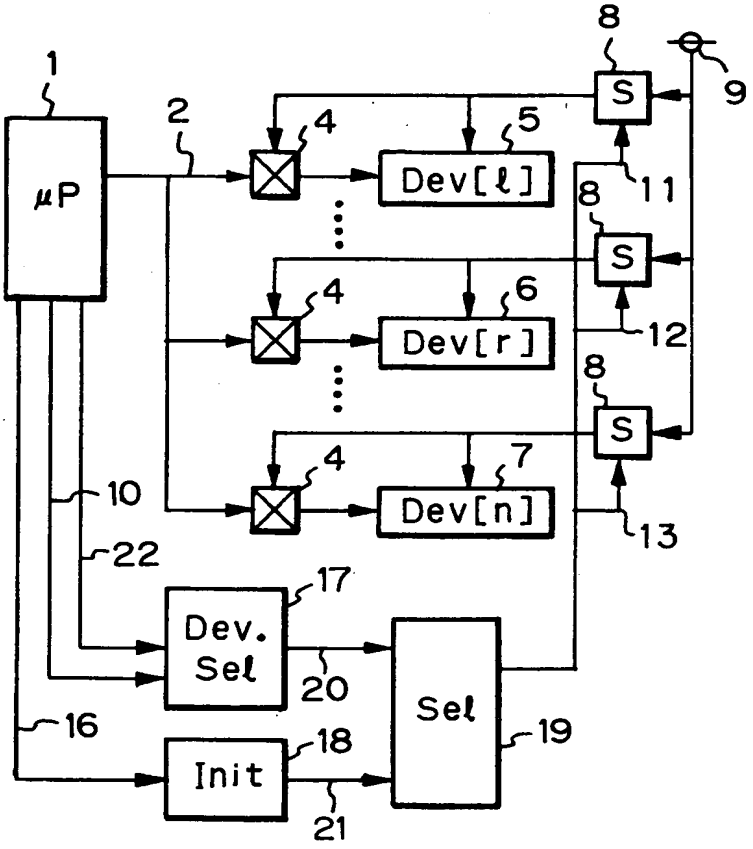
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Fig. 5

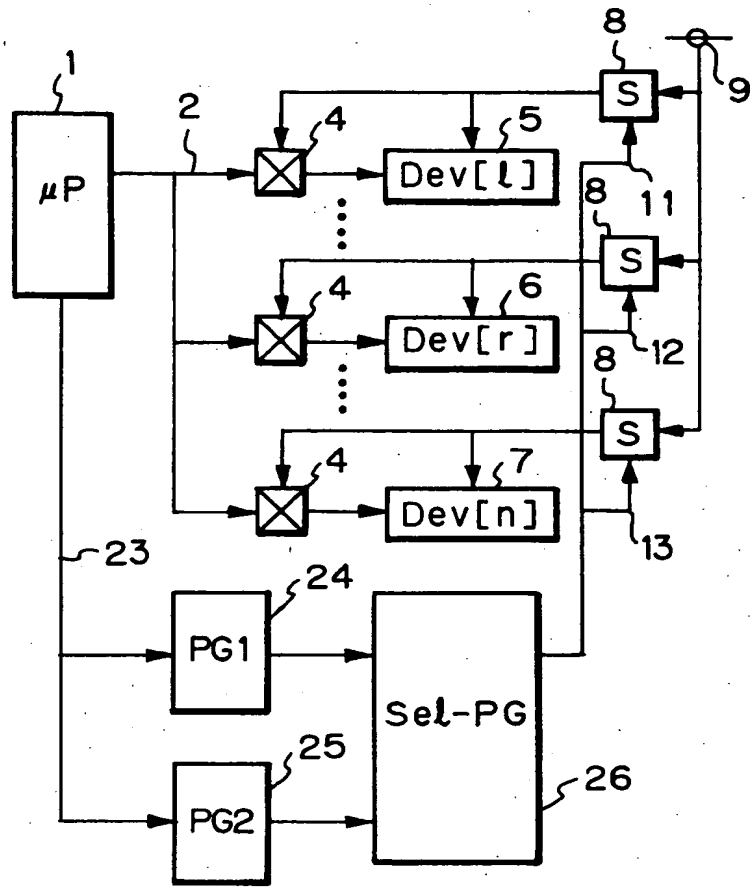
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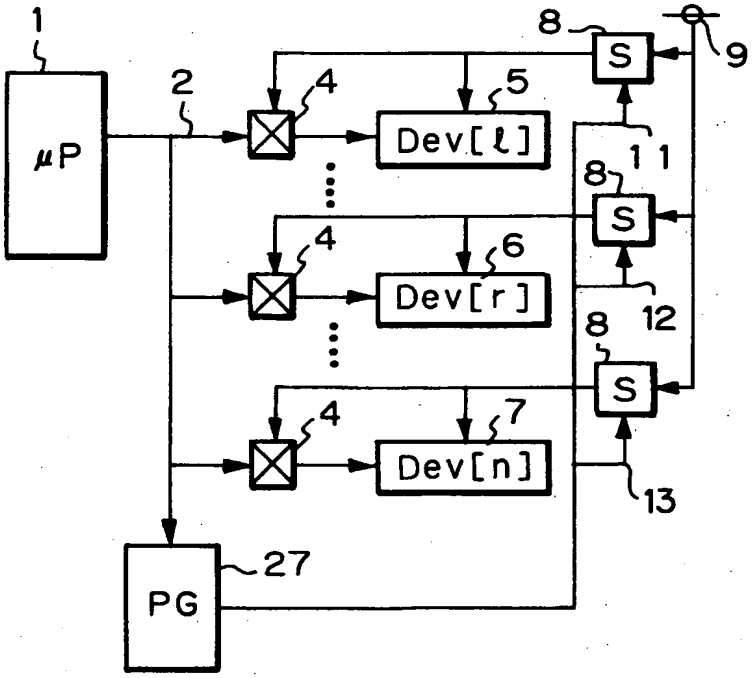
Fig. 6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